DOI: https://doi.org/ 10.15276/aait.02.2019.2
UDC 004.315

POWER-ORIENTED CHECKABILITY AND MONITORING OF THE CURRENT CONSUMPTION IN FPGA PROJECTS OF THE CRITICAL APPLICATIONS

Viktor V. Antoniuk[1)]
ORCID: https://orcid.org/0000-0001-8436-5338, viktor.v.antoniuk@gmail.com
Myroslav O. Drozd[1)]
ORCID: https://orcid.org/0000-0003-0770-6295, miroslav_dr@mail.ru
Oleksandr B. Drozd[1)]
ORCID: https://orcid.org/0000-0003-2191-6758, drozd@ukr.net
[1)] Odessa National Polytechnic University. 1, Shevchenko Avenue. Odesa, 65044, Ukraine

ABSTRACT

The article is devoted to the problem of checkability of the circuits as an essential element in ensuring the functional safety of informational and control safety-related systems that monitoring objects of increased risk in the energy, transport, military, space and other industries to prevent accidents and reduce their consequences occurrence. The key role of checkability in the transformation of fault-tolerant structures used in such systems into fail-safe ones is noted. The problems of logical checkability are shown, including the problem of hidden faults, inherent for safety-related systems in the modern design of its components using matrix structures. It was proposed to supplement logical checkability with other forms, among which the most promising are power-oriented checkability, supported by the successful development of green technologies in FPGA (Field Programmable Gate Array) design. The problems of limited accuracy in the assessment and measurement of temperature, which manifested themselves in the development of thermal testability and thermal methods for monitoring circuits, are noted. The lower and upper power-oriented checkability of the circuits is determined by the current consumption parameter. Analytical estimates of the lower and upper checkability of the circuits by current consumption were obtained considering the peculiarities of their design on FPGA using modern CAD (Computer-Aided Design) using the example of Quartus Prime Lite 18.1. The threshold values of consumption currents in the methods of monitoring circuits for detecting faults in the chains of common signals and short-circuit faults within the framework of the lower and upper checkability are estimated, respectively. Experiments have been performed, to evaluate the lower and upper power-oriented checkability of the circuits and threshold values for the presented monitoring methods, using the example of a scalable circuit of the shifting register, designed for FPGA. The dependences of the power-oriented lower and upper checkability of the circuits on the occupancy of the FPGA chip are shown.

Keywords: Safety-Related System; FPGA (Field Programmable Gate Array) Design; Power-Oriented Checkability, Monitoring Of Current Consumption, Short-Circuit Fault, Common Signal

***For citation*: Viktor V. Antoniuk, Myroslav O. Drozd, Oleksandr B. Drozd Power-Oriented Checkability and Monitoring of the Current Consumption in FPGA Projects of the Critical Applications. *Applied Aspects of Information Technology.* 2019; Vol.2 No.2: 105–114. DOI: https://doi.org/ 10.15276/aait.02.2019.2**

INTRODUCTION

The most important application of information technologies is the monitoring of high-risk objects, which are widely represented in Ukraine and in the world with powerful power plants, high-speed transport, space and military systems. Information technologies of critical application, implemented in computer instrumentation and control safety-related systems, are a major factor in deterring the risks of man-made disasters. However, the statistics of the occurrence of accidents indicates the need to enhancement technologies to improve the functional safety of critical objects.

Functional security is based on the use of fault-tolerant structures at the system level and its individual components. However, fault tolerance does not guarantee functional safety if the required level of checkability of circuit solutions is not ensured.

In case of its deficiency, the accumulation of hidden faults in an amount, exceeding the capabilities of fault-tolerant circuits, is possible.

The problem is that the limitation in the accumulation of hidden faults is provided mainly by methods and means of logical checking, which identifies the fault by its manifestation in the form of result error in the process of testing digital circuits or in their on-line testing. The logical checking of digital circuits operates within the framework of its corresponding logical checkability, for which, at the present stage of development of safety-related systems, there is objectively exist a problem of hidden faults. To limit the accumulation of faults in safety-related systems, it is necessary to supplement the logical checkability with other forms.

The successful progress of green technologies and FPGA design in the development of components for safety-related systems identifies power-based forms as promising.

The aim of the work is to analyze the problems of logical checkability that stimulate the development of other forms, and, as a result, the development of power-oriented checkability of FPGA projects and monitoring energy consumption of the components of safety-related systems, based on it.

To achieve this goal, the following tasks are solved.

1) A review of the current level of logical checkability in critical applications and the reasons for its limitations is conducted.

2) The concept of power-oriented checkability is developed, its types that provide monitoring of current consumption to detect faults in chains of common signals and short-circuit faults, are determined and evaluated analytically.

3) Experiments are being conducted to evaluate the power-oriented checkability of scaled FPGA projects using the example of a shifting register circuit.

RELATED WORKS

The development and operation of informational and control safety-related systems is governed by international standards in the direction of ensuring functional safety of both the system and the critically control object to prevent accidents and reduce losses in the event of their occurrence [1, 2].

The risk in the area of critical infrastructures is estimated by the multiplication of the probability of an incident and the cost of the consequences, which are directly related to the quantitative and qualitative development of control objects. Therefore, the containment of risks requires a constant decrease in the probability of an accident, i.e. improve safety-related systems in ensuring functional safety [3, 4].

Safety-related systems differ from conventional computers in designing for operation in two modes: normal and emergency. The functioning of the digital components of the system in these modes, as a rule, differs by input data [5, 6].

In testing, the logical checkability of digital circuits is represented by testability, which is structural in nature, i.e. determined only by the structure of the circuit [7, 8].

In on-line testing, logical checkability gains dependence on input data and becomes structurally functional. In critical systems, structurally functional checkability is converted to dual-mode, i.e. different in normal and emergency modes due to different input data [9].

Duplication of logical checkability in safety-related systems occurs under conditions of low structurally functional checkability of digital circuits in normal mode. This leads to the problem of hidden faults that can accumulate in the circuits over the course of an extended normal mode in the absence of input data that manifest them. Accumulated faults present a real threat to the fault tolerance of digital circuits in emergency mode, since they can appear on the emergency input data in an amount that exceeds their parry capabilities [10].

The lack of confidence in the fault tolerance of the circuits is manifested in the use of hazardous imitation modes, which, for the sake of increasing checkability, recreate emergency conditions and often lead to them as a result of unauthorized switching by person or malfunction [11, 12].

In addition, a lack of confidence in digital circuit fault tolerance indicates an insufficient level of their logical checkability, which does not allow fault-tolerant solutions to provide functional safety for digital components of safety-related systems.

The low structurally functional logical checkability of digital circuits in the normal mode is characteristic of the current level of development of safety-related systems in their components. The main reason for this drawback is the design of digital circuits using matrix structures: parallel adders and shifters, an iterative array of multipliers and dividers [13, 14].

Matrix structures, as they grow, reduce the controllability and observability of internal connections of the digital circuit and in this way significantly reduce its testability, which is the upper limit of structurally functional checkability, and that, in turn, is the upper limit of two-mode structurally functional checkability of the circuits [15].

At the present time, matrix structures dominate in the development of computing. With all their shortcomings, this dominance takes a protracted nature, because in the past decades a powerful infrastructure has been created in support of matrix structures. Methods of design of digital components, modern CAD, element base, all of them are focused on design using matrix structures [16, 17].

Therefore, the existing lack of logical checkability must be filled with the development of other forms of checkability and appropriate control methods, among which it is advisable to single out power-oriented approaches.

The success achieved in the development of green technologies and their use in modern CAD systems, including FPGA design, testifies in their favor [18, 19].

It should also be noted their advantages such as improving the energy characteristics with the complexity of the schemes, which favorably differs from logical checkability, which in this case decreases. In addition, power-oriented checkability is not limited to digital circuits as a logical form, but also applies to hybrid and analog circuits [20, 21].

ISSN 2617-4316 (Print)
ISSN 2663-7723 (Online)

In power-oriented approaches to the development of checkability of circuits and control methods, the focus is on exploring the possibilities of detecting faults in terms of power dissipation, which is manifested in temperature estimates. This is due to the availability of temperature measurement with appropriate sensors in terms of price and their diversity. Research and practice of use cover the areas of circuit design in the direction of ensuring and improving thermal testability [22], as well as the development of on-line thermal monitoring methods [23].

This direction is being developed in FPGA design. CAD systems that support FPGA design contain utilities that simulate the circuits for their power dissipation and the corresponding crystal temperature. FPGA chips use internal and external temperature sensors. However, at present time, the accuracy of temperature assessment by the utility and measurement by sensors is at the level of 0.5 °C. This significantly limits the ability to detect circuit faults in terms of power dissipation and temperature values. More accurate data on power parameters and their change by faults can be obtained from simulation results performed by utilities, as well as from sensors in terms of current consumption, characterizing power consumption at a constant supply voltage [24, 25].

TYPES OF POWER-ORIENTED CHECKABILITY AND THEIR EVALUATION

The checkability is based on the division of the values of the monitored code or parameter into two sets or two areas of possible and impossible values: values that can be with the correct functioning of the circuit, and values that occur only under the action of a fault. Logical checkability operates with the concept of a set of values of a controlled code, and power-oriented checkability - with an area of values of a monitored parameter. This area is represented by a range of values, i.e. characterized by the smallest and largest parameter value.

Quantitative assessment of checkability relates the capacity of a set or the volume of a range of impossible values, i.e. their quantity, to the entire quantity of possible and impossible values. This assessment allows you to compare the circuits according to their inherent ability to identify faults.

The code control method in the case of logical checkability or the method of monitoring the values of the controlled parameter in a power-oriented form detects faults within the specified circuit capability. In the case of power-oriented checkability, the ability of the method to detect faults is also limited by the measurement error of the parameter.

In the power-oriented checkability the parameter is power for which the range of possible values lies between two areas of impossible values: lower and higher. Therefore, checkability is represented as lower and higher, which are described using the lower and higher areas of impossible values. Monitoring methods that detect faults in these areas of impossible values are limited to the minimum and maximum possible values of the parameter, respectively.

Power can be represented in two manifestations: as consumed or dissipated.

The dissipated power is estimated from the temperature indications, and, as noted above, is measured with limited accuracy. The consumed power is estimated by the current consumption, taking into account the constant voltage, and is measured with an error in hundredths of a percent. This significantly brings the capabilities of the power monitoring method to the power-oriented checkability. The following describes the checkability and power monitoring methods by current consumption.

Lower checkability, which characterizes the ability to control faults that reduce current consumption, in particular, faults in the chains of common signals, can be estimated by the formula:

$$C_L = I_{D\,MIN} / I_{D\,MAX}, \quad (1)$$

where $I_{D\,MIN}$, $I_{D\,MAX}$ – minimum and maximum possible dynamic components of current consumption, respectively.

The current consumption I_T of a project on FPGA consists of the sum of a dynamic I_D and a static I_S components. The static component is determined by the consumption of chip components and leakage currents, and the dynamic component is determined by the activity of signals in a project. Analysis of lower checkability shows that it is related to the dynamic component of the current consumption. Faults in the chains of common signals can lead to blocking of a part of the circuit by a violation of synchronization or general control signals, that significantly reducing the number of switching of information signals. This leads to a decrease in the dynamic component of the current consumption.

To monitor common signals, the minimum permissible threshold of the dynamic component $I_{D\,MIN}$ of the current consumption of the project is important. The threshold is determined at zero activity of the project information signals, i.e. when dynamic power consumption is entirely determined by the synchronization signals.

During the operation of the FPGA project, the consumed current sensor measures its value I_M,

which determines the dynamic component of the measurement $I_{MD} = I_M - I_S$, where I_S – is the static component, which is determined in the process of preliminary modeling by the utility in the CAD system. Simulation and measurement errors can slightly increase the value of I_{MD} (by 0,01 % – 0,02 %).

The method of monitoring consumed current detects faults in the chains of common signals when the condition $I_{MD} < I_{D\,MIN}$ is met.

The dynamic component $I_{D\,MAX}$ is determined at the maximum possible switching frequency of information signals, which for the proper functioning of the project should not exceed 100 % of the synchronization frequency. For real projects, as a rule, the activity of information signals is much less than the activity of a synchronization signal, and ranges from 10 to 20 %. The modeling of the parameters of power consumption and heat dissipation of the project is performed by the appropriate CAD tool for the default activity of information signals at the level of 12,5 % of the sync signal.

Higher checkability of circuit supports the control of faults that increase the current consumption, which is typical for short-circuit faults, and can be estimated by the formula:

$$C_H = (I_B - I_{MAX}) / (I_B - I_{MIN}), \qquad (2)$$

where: I_B, I_{MAX}, I_{MIN} – bordering, maximum and minimum values of the possible current consumption, respectively.

The current I_B is determined individually for each project, based on the maximum possible signal activity for it. This activity exceeds the bordering values of the synchronization frequencies for the correct functioning of the project and determines the physically permissible limit of the dynamic current consumption, the excess of which leads to violation of the operating parameters of the chip, in particular, the maximum temperature of the crystal.

The method of monitoring short-circuits for power consumption consists in determining for a particular project the maximum allowable (threshold) value of the current consumed, achieved with proper operation with the maximum possible activity of internal and input / output signals. Obviously, in the case of register schemes, this activity cannot exceed the synchronization frequency in the case of proper operation.

Thus, the threshold value of the consumed current I_{MAX} is determined based on two parameters of the project:

- The maximum possible clock frequency of synchronization signal;
- The maximum possible activity of the project information signals, which for its proper functioning should not exceed 100 % of the synchronization signal.

The current I_{MAX} is calculated when determining the energy parameters of the project in the process of modeling in CAD, is reduced by the value of the modeling error (0,01 %) and compared during the operation of the circuit with the value of the operating current I_M of the circuit, that received from the sensor. The method of monitoring the consumed current detects a short-circuit fault when the condition $I_M > I_{MAX}$ is met.

The I_{MIN} current is determined for the project at the minimum, i.e. zero, input / output and internal signals activity.

EXPERIMENTAL PART

An experimental assessment of the checkability that is energy-oriented in terms of the current consumption parameter was carried out for the design of a shift register with an inverter located at the output of each bit.

A fragment of the shift register circuit for two bits is shown in Fig. 1.

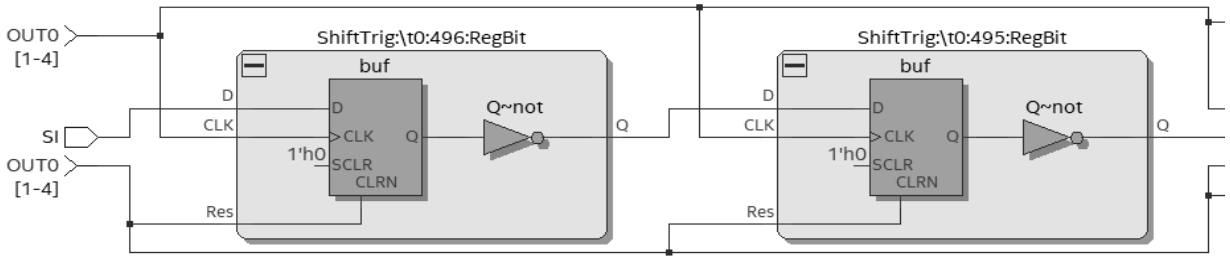


Fig. 1. **Shift register**
Source: **compiled by the authors**

ISSN 2617-4316 (Print)
ISSN 2663-7723 (Online)

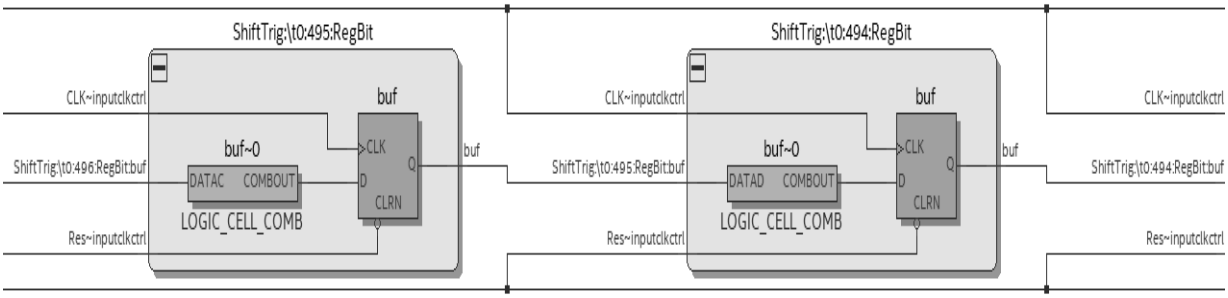
The implementation was carried out on FPGA Intel Max 10 10M50DAF672I7G [26]. The simulation was performed in the Quartus Prime Lite 18.1 CAD system [27]. The energy parameters of the design were estimated using the PowerPlay Power Analyzer utility [28].

The logical element, consisting of the logical table LUT and the trigger, is the main architectural component of the FPGA. The matrix of logic elements and switched connections between them makes up to 85 % of the chip area. When implementing a shift register circuit, each register bit occupies one logical element, which contains a trigger used to save the bit value of the current bit, and the LUT table to implement the inversion function of the previous bit.

An example of placing two bits of a shift register on an FPGA is shown in Fig. 2.

Fig. 2. **Placing two bits of the shift register on the FPGA**

Source: **compiled by the authors**



The checkability of the circuits by current consumption for faults in the chains of common signals and short-circuits was evaluated depending on the occupancy of the FPGA chip. For this, the design of the shift register was scaled by designing circuits with an increase in bit width using 1 %, 10 %, 20 %, 40 % and 80 % of the total number of logic elements, which for the selected FPGA chip is 49760.

An example of a 40 % fill-up of an FPGA chip is shown in Fig. 3.

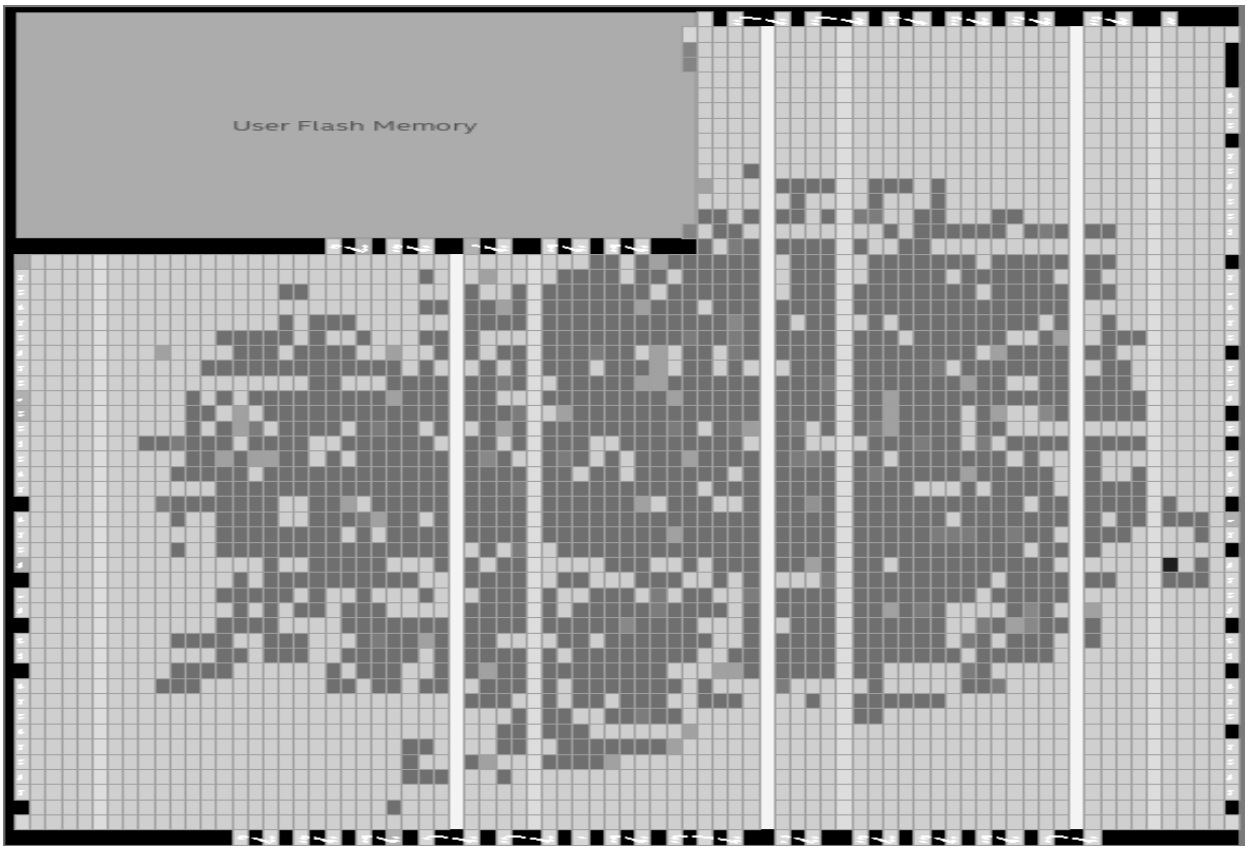


Fig. 3. **FPGA chip capacity example**

Source: **compiled by the authors**

To establish the dependence of checkability of common signals by current consumption from the FPGA chip occupancy, the total current consumption I_T, as well as its dynamic I_D and static I_S components for cases of 0, 12,5 % and 100 % of the information signals activity were obtained by modeling using the Power Play Power Analyzer utility for each scaled shift register design.

The values of checkability C_L were calculated by the formula (1) for each of the scaled design and the cases when $I_{D\,MAX}$ is set with the activity of information signals at 100 % and 12,5 %. The results of the experiments are presented in Table 1.

Table 1. **The results of experiments to assess checkability C_L**

Percentage of used logical elements	Activity of information signals in % from synchronization signal	Core current consumption, *mA*			Checkability C_L, %	
		I_T	I_D	I_S	At 100 % activity of information signals	At 12,5 % activity of information signals
1 %	0 %	28,85	17,07	11,78	41	85
	12,5 %	31,99	20,20	11,80		
	100 %	53,98	42,08	11,89		
10 %	0 %	80,75	68,77	11,98	22	70
	12,5 %	110,61	98,51	12,09		
	100 %	319,64	306,72	12,92		
20 %	0 %	141,02	128,82	12,21	21	68
	12,5 %	201,08	188,64	12,44		
	100 %	621,55	607,38	14,17		
40 %	0 %	251,81	239,17	12,64	20	67
	12,5 %	371,98	358,86	13,12		
	100 %	1213,59	1196,72	16,88		
80 %	0 %	450,48	437,04	13,43	19	65
	12,5 %	690,76	676,31	14,45		
	100 %	2374,60	2351,20	23,40		

Source: **compiled by the authors**

The table shows a high level of power-oriented checkability of common signals with a standard level of activity of information signals and its decrease with an increase in the chip occupancy and in the activity of information signals.

The simulation performed using the Power Play Power Analyzer utility determined the minimum I_{MIN} and maximum I_{MAX} current values, as well as the bordering current I_B for each version of the scaled design. Values were estimated by setting the maximum possible switching frequency of the design's circuit signals. In this case, the crystal temperature reaches the maximum permissible value of 100 °C.

The maximum synchronization signal frequency, according to the estimates of the Power Play Power Analyzer utility, was 250 MHz for all scaled designs.

The results of the experiments are presented in Table 2, where for each scaled design of the shift register are given the corresponding values of the maximum switching frequency of signals, consumed currents I_B, I_{MAX}, I_{MIN} and the values of checkability C_H, that calculated by formula (2).

***Table 2*. The results of experiments to assess checkability C_H**

Percentage of used logical elements	Maximum switching frequency of signals, millions of transitions / sec.	Consumed current, *mA*			Checkability C_H, %
		I_B	I_{MAX}	I_{MIN}	
1 %	30000	4450,57	49,28	25,10	99
10 %	6600	7708,30	319,64	80,75	97
20 %	3300	7863,57	621,55	141,02	94
40 %	1700	7972,12	1213,59	251,81	88
80 %	880	8102,73	2374,60	450,48	75

Source: **compiled by the authors**

ISSN 2617-4316 (Print)
ISSN 2663-7723 (Online)

The obtained results show a high level of power-oriented checkability of short-circuits and its decrease with increasing chip occupancy due to a decrease in the difference between the bordering I_B and the threshold I_{MAX} current value.

CONCLUSION

The review of the current level of logical checkability of digital circuits showed its shortcomings in solving the problem of hidden faults, which is important for ensuring the functional safety of computer systems in critical applications. This conclusion substantiates the development of other forms of checkability, among which the power-oriented form receives substantial support from modern CAD systems in the development of FPGA projects using the achievements of green technologies.

The obtained estimates of the lower and upper checkability showed the high potential of this form for monitoring the current consumption of circuits in order to detect hidden faults in the chains of common signals and short-circuits based on changes in the consumed current beyond the limits of proper operation.

The performed experiments confirmed the high level of the studied lower and upper checkability of the circuits in terms of the current consumption parameter in the conditions of different chip occupancy.

REFERENCES

1. IEC 61508:2010 “Functional Safety of Electrical / Electronic / Programmable Electronic Safety-related Systems”. 2010.

2. Andrashov, A., Kharchenko, V., Siora, A., Sklyar, V. & Volkoviy, A. “A Certification of FPGA-based safety Instrumentation and Control platform in accordance with IEC 61508”. *Critical Infrastructure Safety and Security.* Kirovograd: Ukraine. 2011; Vol. 1: 148–152.

3. Brezhnev, E. “Risk-analysis in critical informational control system based on computing with words’ models”. *VII International workshop of Digital Technologies.* Zilina: *Slovak Republic.* 2010. p. 19–20.

4. Ivanchenko, O., Kharchenko, V., Moroz, B., Kabak, L. & Konovalenko, S. “Risk Assessment of Critical Energy Infrastructure Considering Physical and Cyber Assets: Methodology and Models”. *International Conference on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications.* 2018. p. 225–228.

5. “Core Knowledge on Instrumentation and Control Systems in Nuclear Power Plants”, Technical Reports, IAEA Nuclear energy series. *International atomic energy agency. Vienna.* 2011; No.NP-T-3.12: 141 p.

Kharchenko, V., Bakhmach, E., Siora, A., Sklyar, V. & Tokarev, V. “Diversity-Oriented FPGA-Based NPP I&C Systems: Safety Assessment, Development, Implementation”. *18th International Conference on Nuclear Engineering.* Xi’an: China. 2010; Vol. 1: p. 755–764. DOI: https://doi.org/10.1115/ICONE18-29754.

6. Bennets, R. G., Maunder, C. M. & Robinson, G. D. “CAMELOT: a computer-aided measure for logic testability,” *IEE Proceedings E-Computers and Digital Techniques.* 1981; Vol.128 No.5: 177–189.

7. Matrosova, A., Nikolaeva, E., Kudin, D. & Singh, V. “PDF testability of the circuits derived by special covering ROBDDs with gates”, *IEEE East-West Design and Test Symposium, EWDTS.* Rostov-on-Don, Russian Federation. 2013. p. 1–5.

Drozd, A., Kuznietsov, M., Antoshchuk, S., Martynyuk, A., Drozd, M. & Sulima, J. “Evolution of a Problem of the Hidden Faults in the Digital Components of Safety-Related Systems”. *16th IEEE East-West Design & Test Symposium.* 2018. p. 1–5. DOI: https://doi.org/10.1109/EWDTS.2018.8524806.

Drozd, M. & Drozd, A. “Safety-Related Instrumentation and Control Systems and a Problem of the Hidden Faults”. *The 10th International Conference on Digital Technologies 2014.* Zhilina: Slovak Republic. 2014. p. 137–140. DOI: https://doi.org/10.1109/DT.2014.6868692.

8. Gillis, D. “The Apocalypses that Might Have Been”. – Available from: https://www.damninteresting.com/the-apocalypses-that-might-have-been/. – Active link – 2019.03.20.

9. “U.S.-Canada Power System Outage Task Force”: Final Report on the August. 14. 2003 Black-out in the United States and Canada: Causes & Recommendations USA.

10. Pham, D. “Overview of the architecture, circuits design and physical implementation of the first-generation Cell processor”. *IEEE J. Solid-State Circuits.* 2007; Vol. 41, No. 8: 1692–1705.

Drozd, J., Drozd, A., Antoshchuk, S., Kushnerov, A. & Nikul, V. “Effectiveness of Matrix and Pipeline FPGA-Based Arithmetic Components of Safety-Related Systems”. *8th IEEE International Conference on*

Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications, Warsaw: Poland. 2015. p. 785–789. DOI: https://doi.org/10.1109/IDAACS.2015.7341410.

Drozd, A., Antoshchuk, S., Drozd, J., Zashcholkin, K., Drozd, M., Kuznietsov, N., Al-Dhabi, M. & Nikul, V. "Checkable FPGA Design: Energy Consumption, Throughput and Trustworthiness". In book: Green IT Engineering: Social, Business and Industrial Applications, Studies in Systems, Decision and Control. V. Kharchenko, Y. Kondratenko, J. Kacprzyk (edits). *Springer International Publishing* 2018; Vol. 171: 73–94. Berlin: Heidelberg. DOI: https://doi.org/10.1007/978-3-030-00253-4_4.

11. "Intel FPGA Integer Arithmetic IP Cores User Guide". – Available from: https://www.intel.com/content/dam/www/programmble/us/en/pdfs/literature/ug/ug_lpm_alt_mfug.pdf. – Active link – 2019.03.20.

12. "Xilinx ISE Design Suite". – Available from: https://www.xilinx.com/products/design-tools/ise-design-suite.html. – Active link – 2019.03.20.

13. Kharchenko, V., Gorbenko, A., Sklyar, V. & Phillips, C. "Green Computing and Communi-cations in Critical Application Domains: Challenges and Solutions". *9th International Conference on Digital Technologies (DT'2013)*. Zhilina: Slovak Republic. 2013. p. 191–197.

Palagin, A. V., Opanasenko, V. N. & Kryvyi, S. L. "Resource and Energy Optimization Oriented Development of FPGA-Based Adaptive Logical Networks for Classification Problem". In book: Green IT Engineering: Components, Networks and Systems Implementation. V. Kharchenko, Y. Kondratenko, J. Kacprzyk (Eds.). Vol. 105. Berlin: Heidelberg: *Springer International Publishing*. 2017. p. 195–218. DOI: https://doi.org/10.1007/978-3-319-55595-9_10.

14. "Xilinx analog mixed signal solutions". WP392 (v1.1). – Available from: https://www.xilinx.com/support/ documentation/white_papers/wp392-analog-mixed-signal.pdf. – Active link – 2019.03.20.

15. "Anadigm Field Programmable Analog Arrays". – Available from: https://www.anadigm.com/fpaa.asp. – Active link – 2019.03.20.

16. Székely, V., Márta, Cs., Rencz, M., Benedek, Zs. & Courtois, B. "Design for Thermal Testability (DFTT) & a CMOS Realization". *1st Therminic Workshop, Grenoble,* France: 1995.

Székely, V., Rencz, M., Karam, J.M., Lubaszewski, M. & Courtois, B. "Thermal Monitoring of Self-Checking Systems". *Journal of Electronic Testing.* 1998; Vol.12 Issue 1-2: 81–92. DOI: https://doi.org/10.1023/A:1008233907036.

17. "PowerPlay Power Analysis". Quartus II Handbook Version 13.1.0. Altera Corporation. – Available from: http://www.altera.com/literature/hb/qts/qts_qii53013.pdf. – Active link – 2019.03.20.

18. "MAX 10 FPGA Development Kit User Guide". – Available from: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug-max10m50-fpga-dev-kit.pdf. – Active link – 2019.03.20.

19. "MAX 10 FPGA Device Architecture". – Available from: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/max-10/m10_ architecture.pdf. – Active link – 2019.03.20.

20." Intel Quartus Prime Standard Edition User Guide: Getting Started". – Available from: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug-qps-getting-started.pdf. – Active link – 2019.03.20.

21. "Intel Quartus Prime Standard Edition User Guide: Power Analysis and Optimization". – Available from:: https://www.intel.com/content/www/us/en/programmable/documentation/ xhv1529966780595.html. – Active link – 2019.03.20.

Conflicts of Interest: the authors declare no conflict of interest

Received 25.03.2019
Received after revision 19.04.2019
Accepted 22.04. 2019

DOI: https://doi.org/10.15276/aait.02.2019.2
УДК 004.315

ЕНЕРГО-ОРІЄНТОВАНА КОНТРОЛЕПРИДАТНІСТЬ ТА МОНІТОРИНГ

ISSN 2617-4316 (Print)
ISSN 2663-7723 (Online)

СПОЖИВАНОГО СТРУМУ В FPGA ПРОЕКТАХ КРИТИЧНИХ ДОДАТКІВ

Віктор Вікторович Антонюк[1)]
ORCID: https://orcid.org/ 0000-0001-8436-5338, viktor.v.antoniuk@gmail.com
Мирослав Олександрович Дрозд[1)]
ORCID: https://orcid.org/0000-0003-0770-6295, miroslav_dr@mail.ru
Олександр Валентинович Дрозд[1)]
ORCID: https://orcid.org/0000-0003-2191-6758, drozd@ukr.net
[1)] Одеський національний політехнічний університет, пр. Шевченко, 1. Одеса, 65044, Україна

АНОТАЦІЯ

Статтю присвячено проблемі контролепридатності схем як істотного елементу у забезпеченні функціональної безпеки інформаційних управляючих систем критичного застосування, що виконують моніторинг об'єктів підвищеного ризику в енергетиці, на транспорті, у військовій, космічній та інших галузях для запобігання аварій і зниження їх наслідків у разі виникнення. Відзначається ключова роль контролепридатності в трансформації відмовостійких структур, які використовуються в таких системах, в відмовобезпечні. Показані проблеми логічної контролепридатності, включаючи проблему прихованих несправностей, притаманну системам критичного застосування при сучасному проектуванні їх компонентів з використанням матричних структур. Запропоновано доповнювати логічну контролепридатність іншими формами, серед яких до найбільш перспективних віднесена енерго-орієнтована контролепридатність, підтримана успішним розвитком зелених технологій в FPGA (Field Programmable Gate Array) проектуванні. Відзначено проблеми обмеженої точності в оцінці та вимірюванні температури, що проявилися в розвитку термальної тестопригодності і термальних методів моніторингу схем. Визначена нижня і верхня енерго-орієнтована контролепридатність схем по параметру споживаного струму. Отримано аналітичні оцінки нижньої і верхньої контролепридатності схем по споживаному струму з урахуванням особливостей їх проектування на FPGA з використанням сучасних CAD (Computer-Aided Design) на прикладі Quartus Prime Lite 18.1. Оцінені порогові значення струмів споживання в методах моніторингу схем для виявлення несправностей в ланцюгах загальних сигналів і несправностей короткого замикання в межах нижньої і верхньої контролепридатності, відповідно. Були проведені експерименти з оцінки нижньої і верхньої енерго-орієнтованої контролепридатності схем і порогових значень для представлених методів моніторингу на прикладі спроектованої на FPGA масштабованої схеми зсувного регістру. Показані залежності енерго-орієнтованої нижньої і верхньої контролепридатності схем від заповнюваності FPGA чіпа.

Ключові слова: системи критичного застосування; FPGA (Field Programmable Gate Array) проектування; енерго-орієнтована контролепридатність; моніторинг споживаного струму; короткі замикання; загальні сигнали

DOI: https://doi.org/10.15276/aait.02.2019.2
УДК 004.315

ЭНЕРГО-ОРИЕНТИРОВАННАЯ КОНТРОЛЕПРИГОДНОСТЬ И МОНИТОРИНГ ПОТРЕБЛЯЕМОГО ТОКА В FPGA ПРОЕКТАХ КРИТИЧЕСКИХ ПРИЛОЖЕНИЙ

Виктор Викторович Антонюк[1)]
ORCID: https://orcid.org/0000-0001-8436-5338, viktor.v.antoniuk@gmail.com
Мирослав Александрович Дрозд[1)]
ORCID: https://orcid.org/0000-0003-0770-6295, miroslav_dr@mail.ru
Александр Валентинович Дрозд[1)]
ORCID: https://orcid.org/0000-0003-2191-6758, drozd@ukr.net
[1)] Одесский национальный политехнический университет, пр. Шевченко, 1. Одесса, 65044, Украина

АННОТАЦИЯ

Статья посвящена проблеме контролепригодности схем как существенного элемента в обеспечении функциональной безопасности информационных управляющих систем критического применения, выполняющих мониторинг объектов повышенного риска в энергетике, на транспорте, в военной, космической и других отраслях для предотвращения аварий и снижения их последствий в случае возникновения. Отмечается ключевая роль контролепригодности в трансформации отказоустойчивых структур, используемых в таких системах, в отказобезопасные. Показаны проблемы логической контролепригодности, включая проблему скрытых неисправностей, присущую системам критического применения при современном проектировании ее компонентов с использованием матричных структур. Предложено дополнять логическую контролепригодность другими формами, среди которых к наиболее перспективным отнесена энерго-ориентированная контролепригодность, поддержанная успешным развитием зеленых технологий в FPGA (Field Programmable Gate Array) проектировании. Отмечены проблемы ограниченной точности в оценке и измерении температуры, проявившиеся в развитии термальной тестопригодности и термальных методов мониторинга схем. Определена нижняя и верхняя энерго-

ориентированная контролепригодность схем по параметру потребляемого тока. Получены аналитические оценки нижней и верхней контролепригодности схем по потребляемому току с учетом особенностей их проектирования на FPGA с использованием современных CAD (Computer-Aided Design) на примере Quartus Prime Lite 18.1. Оценены пороговые значения токов потребления в методах мониторинга схем для обнаружения неисправностей в цепях общих сигналов и неисправностей короткого замыкания в рамках нижней и верхней контролепригодности, соответственно. Проведены эксперименты по оценке нижней и верхней энерго-ориентированной контролепригодности схем и пороговых значений для представленных методов мониторинга на примере спроектированной на FPGA масштабируемой схемы сдвигового регистра. Показаны зависимости энерго-ориентированной нижней и верхней контролепригодности схем от заполняемости FPGA чипа.

Ключевые слова: системы критического применения; FPGA (Field Programmable Gate Array) проектирование; энерго-ориентированная контролепригодность; мониторинг потребляемого тока; короткие замыкания; общие сигналы

ABOUT THE AUTHOR

Viktor V. Antoniuk, Master, Senior Lecturer of Computer Intellectual Systems and Networks Department. Odessa National Polytechnic University, 1, Shevchenko Avenue. Odesa, 65044, Ukraine
ORCID: https://orcid.org/0000-0001-8436-5338, viktor.v.antoniuk@gmail.com
***Research field*:** On-Line Testing of the Digital Components; FPGA-Based Systems

Віктор Вікторович Антонюк, магістр, старший викладач кафедри Комп'ютерних інтелектуальних систем і мереж. Одеський національний політехнічний університет, пр. Шевченко, 1, Одеса, 65044, Україна

Myroslav O. Drozd, PhD (Eng), Senior Lecturer of Information Systems Department. Odessa National Polytechnic University, 1, Shevchenko Avenue. Odesa, 65044, Ukraine
ORCID: https://orcid.org/ 0000-0003-0770-6295, miroslav_dr@mail.ru
***Research field*:** On-Line Testing and Circuit Checkability in the Digital Component of Safety-Related Systems

Мирослав Олександрович Дрозд, кандидат технічних наук, старший викладач кафедри Інформаційних систем. Одеський національний політехнічний університет, пр. Шевченко, 1. Одеса, 65044, Україна

Oleksandr V. Drozd – Dr. Sc. (Eng) (2003), Prof. of Computer Intellectual Systems and Networks Department. OR-CID: https://orcid.org/0000-0003-2191-6758, drozd@ukr.net. Odesa National Polytechnic University, 1, Shevchenko Avenue Odesa, Ukraine
***Research field*:** On-Line Testing; Green Technologies and Circuit Checkability in the Digital Component of Safety-Rlated Systems; LUT-oriented Architecture of FPGA-Based Systems

Олександр Валентинович Дрозд, доктор технічних наук, професор кафедри Комп'ютерних інтелектуальних систем та мереж, Одеський національний політехнічний університет, пр. Шевченка, 1. Одеса, 65044, Україна

ISSN 2617-4316 (Print)
ISSN 2663-7723 (Online)